LOW JITTER DIGITAL FREQUENCY SYNTHESIZER AND CONTROL THEREOF

ABSTRACT OF THE DISCLOSURE

A low jitter digital frequency synthesizer includes a first counter module, a second counter module, a snapshot module, an error value generation module, and a tapped delay line. The first counter module counts intervals of M cycles of an input clock to produce a first count. The second counter module count intervals of D cycles of an output clock to produce a second count, wherein a rate of the output clock corresponds to M/D times a rate of the input clock. The snapshot module periodically takes a snapshot of the first and second counts to produce snapshots. The error value generation module generates an error value based on the snapshots. The tapped delay line module produces the output clock based on the error value.